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# Transient Analysis and Low Power Consumption of Oscillator using C-mos Technology at 90 nm

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## Abstract:

The design and analysis of an oscillator in 90 nm technology using the cadence virtuoso tool. This oscillator has less noise and power consumption. There is also evidence of oscillator periodic steady state response. The portable power supplies, such as solar cells or other devices, it is crucial that electronic devices and circuits that can work at low voltages for portable electronic applications.

**Keywords-** CMOS, oscillator, power consumption, voltage gain, noise analysis.

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**1. INTRODUCTION:** Due to their widespread application in wireless communication, radio frequency integrated circuits (RFICs) have attracted a lot of attention in recent years. One of the crucial RFIC blocks, Phase Locked Loop (PLL), contains the voltage-controlled oscillator. This can be used for everything from frequency synthesizers to transceivers, among other things. One of the active areas of research and development in recent years has been the design of high performances monolithic oscillators. A circuit whose output is a linear function of its control voltage is an ideal oscillator [1]. The oscillator should be built with high gain, low phase noise, and low power consumption to meet the strict requirements of RFIC applications. MOSFETs at higher frequencies have impeded the evolution of low-power designs to RF front-ends. In order to overcome the limitations, various design methodologies and circuit techniques have been proposed [2] – [5]. Among these approaches, low-voltage circuit operation is one of the most promising solutions.

## 2. CIRCUIT ANALYSIS:

Oscillator has a wide tuning range with low power, a large signal swing, a short chip area, and reasonably low phase noise [3, 4]. It is very simple to construct shown by fig. (1)

Two n-mos and 5p-mos, or four mos transistors, are employed in the circuit design. N-mos combine to create an electronic oscillator. The substrates of N1 and N2 are related to one another. The drain of N1 is linked to the source of the p-mos, or P2, and the drain of N2 is connected to the vdd. The source of N2 must be grounded. P2 and N1's gate receive input.

The electronic oscillator is modelled using the following components-

P1 & P2, Model name: gpdk090 – n-mos 1V, length-100nm, total width- 120 nm, threshold -120 nm

N1 & N2 , Model name : gpdk090 – p-mos 1V , length-100nm , total width- 120 nm, threshold-120 nm

Vdd – 0.9 V

Vin – 2 mV

Vsin – amplitude – 1m , frequency – 1 kHz

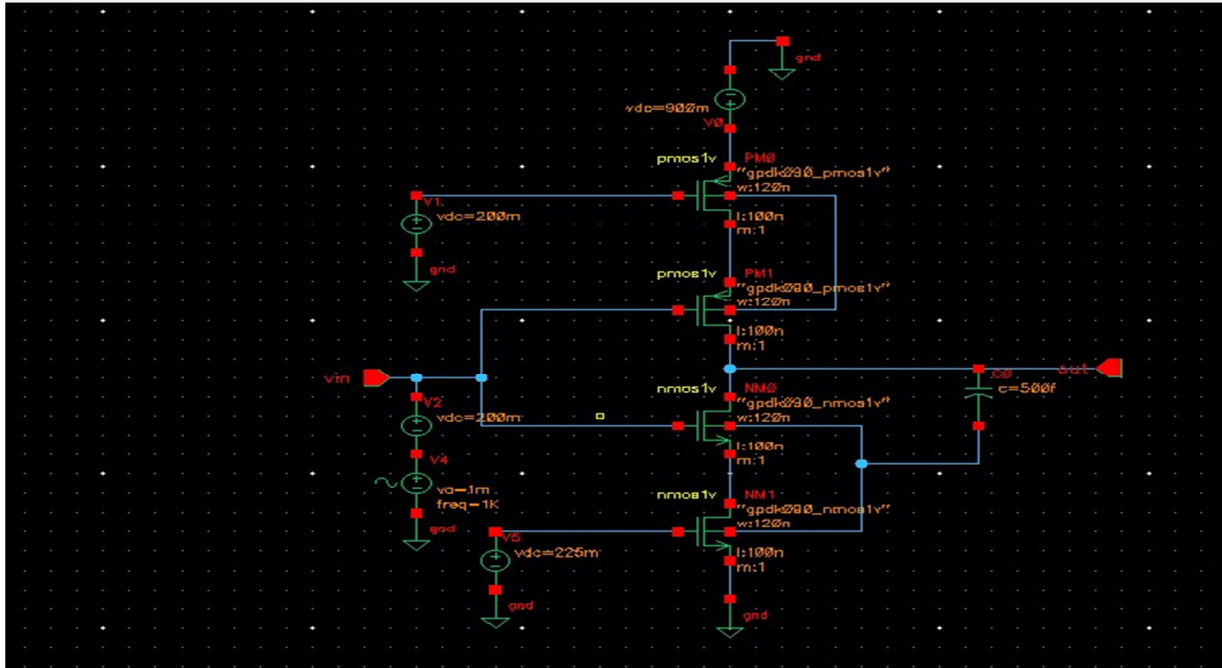


Fig 1- Experimental circuit of electronic oscillator

### 3. DESIGN PARAMETERS AND SIMULATION RESULT OF PROPOSED OSCILLATOR:

The oscillator shows satisfactory transient response with stop time 1 ns fig. (2) , a very low noise response fig. (2) and better gain fig. (4). These are shown by simulation results.

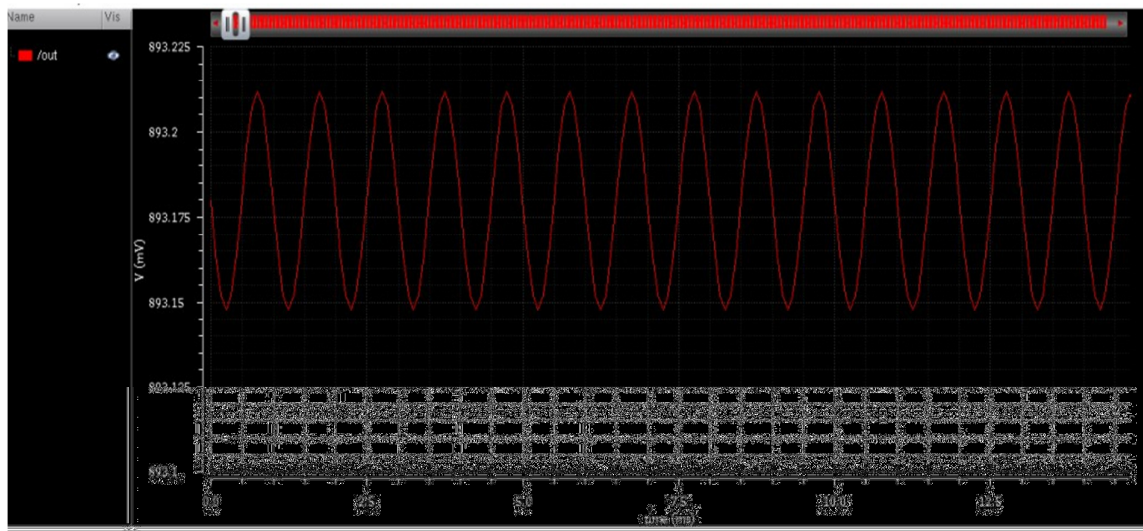


Fig -2 Transient response of proposed oscillator

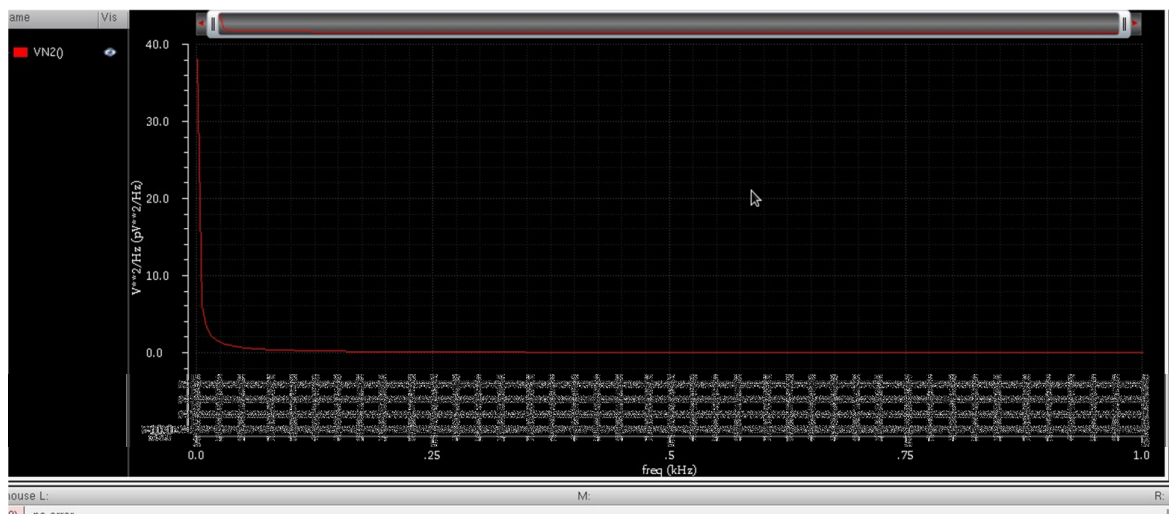


Fig -3 Noise response of proposed oscillator

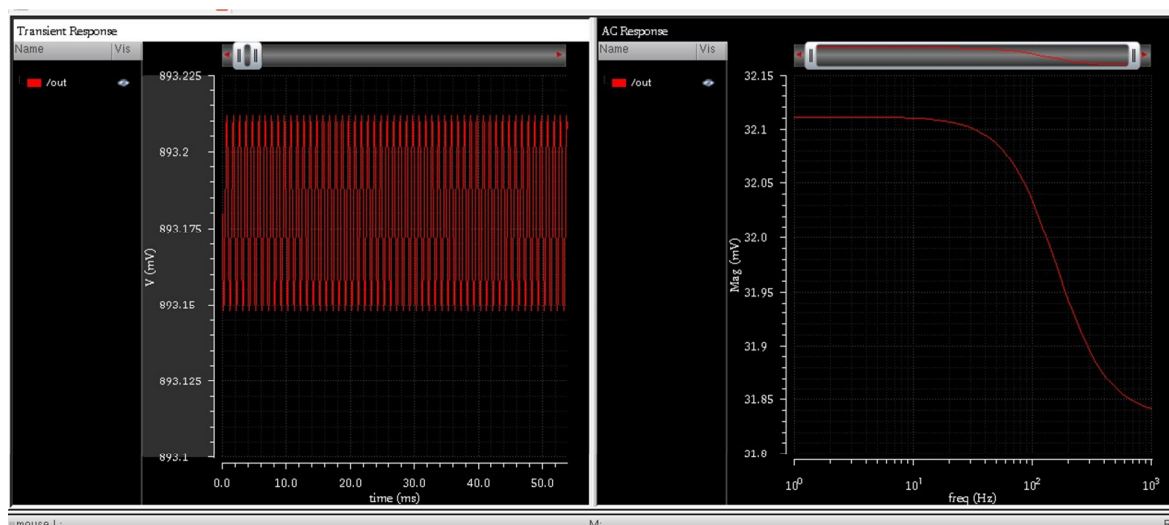


Fig -4 Gain analysis of proposed oscillator

#### 4. CONCLUSION:

In this study, a 90nm CMOS oscillator is built and simulated. The outcomes of the simulation demonstrated that the proposed oscillator structure may outperform existing oscillators in terms of gain. Our suggested design has a high linearity gain in comparison to existing oscillators, which increases the stability of the system. The oscillator with MOS transistors diode linked results in low power consumption, allowing the oscillator to be used for low-voltage low-power applications. Our suggested design has high linearity gain compared to existing oscillators, which increases the system stability, and the oscillator has low power consumption, allowing the oscillator to be used for low-voltage low-power applications.

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***Cite this Article:***

**Nikhata Akhtar, Vaibhav, R.K. Tiwari, "Transient Analysis and Low Power Consumption of Oscillator using C-mos Technology at 90 nm", *International Journal of Scientific Research in Modern Science and Technology (IJSRMST)*, ISSN: 2583-7605 (Online), Volume 2, Issue 6, pp. 87-90, June 2023.**

**Journal URL: <https://ijrmst.com/>**